What is claimed is:

1. A method of routing test signals from test points of an integrated circuit (IC) to output locations comprising:

designating a plurality of the test points in the IC, from which the test signals are generated;

designating a hierarchy of a plurality of regional levels and sub-levels within the IC, each regional level and sub-level including a portion of the test points;

distributing a hierarchy of a plurality of multiplexers across the IC, each multiplexer being local to one of the regional levels and sub-levels;

connecting a lowest-level portion of the multiplexers to the test points to receive the test signals therefrom;

connecting a mid-level portion of the multiplexers to other multiplexers to receive selected portions of the test signals therefrom; and

connecting a highest-level one of the multiplexers to the output locations to supply a final one of the selected portions of the test signals thereto.

2. A method of routing test signals from test points of an integrated circuit (IC) through a plurality of multiplexers to output locations comprising:

arranging the test signals into a plurality of groups;

arranging the groups into a hierarchy of regional levels, including a highest regional level and at least one lower regional level, each regional level corresponding to a region of the IC;

providing a multiplexer for each regional level locally to the region corresponding to the regional level;

selecting one group of test signals by each lower regional level to be passed through the multiplexer thereof to a next higher regional level; and

selecting one group of test signals by the highest regional level to be passed through the multiplexer thereof to the output locations.

3. A method as defined in claim 1 further comprising:

connecting only a portion of the groups of test signals to the multiplexer of the highest regional level.

4. An integrated circuit (IC) comprising:

a plurality of test points from which test signals are generated;

a plurality of output locations at which a portion of the test signals are measured;

a plurality of groups of the test signals;

a plurality of regions within which the test signals are generated and the groups of the test signals are arranged;

a plurality of hierarchical regional levels within which the regions are arranged;

a plurality of multiplexers, each disposed locally to one of the regional levels, at least a portion of the multiplexers connected to receive the groups of the test signals from the test points and at least one of the multiplexers connected to receive at least a portion of the groups of the test signals from another one or more of the multiplexers, each multiplexer selecting one of the groups of the test signals within the regional level to which the multiplexer is locally disposed and passing the selected group of test signals to a next higher regional level or to the output locations;

5. An integrated circuit (IC) comprising:

a plurality of means for generating test signals indicating functioning of the IC;

a plurality of means for outputting selected ones of the test signals;

a plurality of regions relating to functions of the IC;

a plurality of groups of the test signals, the groups being arranged within the regions;

a plurality of hierarchical regional levels within which the regions are arranged;

a plurality of selecting means, each local to one of the regional levels and each for selecting one group of test signals within the regional level to which

the selecting means is local to be passed to the selecting means of a next higher regional level or to the outputting means, at least a portion of the selecting means being connected to the generating means and at least one of the selecting means being connected to the outputting means;

6. An IC as defined in claim 4 wherein each selecting means includes a multiplexer.